

**WHAT IS CLAIMED IS:**

- 1        1.        A method for testing the design of an integrated circuit (system IC)  
2        comprising the steps of:
  - 3                (a) designing the system IC to have a predetermined number and pattern for  
4                its chip I/O pads;
  - 5                (b) designing a packaging module to fan-out the I/O of the system IC to an  
6                expanded pitch of packaging I/O pads having a correspondence to said chip I/O pads;
  - 7                (c) partitioning circuitry of said system IC into a functional circuit;
  - 8                (d) designing said functional circuit as a corresponding test IC, wherein said  
9                test IC I/O pads conform to one of a sub-set of the number and pattern of said chip  
10                I/O pads;
  - 11                (e) attaching said test IC to said packaging module with conductive material;
  - 12                (f) exercising said test IC by applying signals and power to inputs of said  
13                packaging module at packaging I/O pads corresponding to said sub-set of chip I/O  
14                pads; and
  - 15                (g) collecting test data corresponding to said test IC.

- 1        2.     A method for testing the design of an integrated circuit (system IC)  
2        comprising the steps of:  
3                (a) designing said system IC to have a predetermined number and pattern for  
4        its chip I/O pads;  
5                (b) designing a packaging module to fan-out the chip I/O to an expanded pitch  
6        of packaging I/O pads having a correspondence to said chip I/O pads;  
7                (c) partitioning functionality of said system IC into a plurality of individual  
8        functional circuits;  
9                (d) designing said plurality of individual functional circuits as a corresponding  
10       plurality of test ICs, wherein each of the test ICs conforms to one of a plurality of  
11       sub-sets of chip I/O pads making up said number and pattern of said chip I/O pads;  
12                (e) attaching said plurality of test ICs to said packaging module with  
13       conductive material;  
14                (f) interconnecting an I/O of a first test IC of said plurality of test ICs to an  
15       I/O of a second test IC of said plurality of test ICs external to said packaging module;  
16                (g) operating said plurality of test ICs by applying signals and power to  
17       selected ones of said packaging I/O pads corresponding to said plurality of sub-sets of  
18       said number and pattern of said chip I/O pads; and  
19                (h) collecting test data corresponding to operating said plurality of test ICs.
- 1        3.     The method of claim 2 further comprising the steps of:  
2                redesigning a first test IC of said plurality of test ICs generating a redesigned  
3       first test IC in response to said test data;  
4                replacing a corresponding one of said plurality of tests chips with said  
5       redesigned first test IC; and  
6                repeating steps (e)–(g).
- 1        4.     The method of claim 2 further comprising the step of:  
2                redesigning said functionality of said system IC in response to said test data.

- 1        5.        The method of claim 2 further comprising the steps of:  
2                coupling said system IC onto a PCB for a system designed to use said system  
3        IC; and  
4                operating said system IC to emulate at least one function of said system.
- 1        6.        The method of claim 2 further comprising the step of:  
2                testing said system IC in a test fixture designed for said system IC.

1       7.     A test module for a production system IC having a particular number and  
2     pattern of chip I/O pads, comprising:  
3         a test IC corresponding to a sub-set of a total functionality of said system IC,  
4     said test IC having a test IC I/O configuration corresponding to a sub-set of said  
5     particular number and pattern of chip I/O pads;  
6         a packaging module designed for said production system IC, having a  
7     packaging I/O number and pattern of packaging I/O pads for receiving said particular  
8     number and pattern of chip I/O pads;  
9         couplings for electrically coupling said test IC I/O configuration to selected  
10    ones of said packaging I/O pads corresponding to said sub-set of said particular  
11    number and pattern of chip I/O pads; and  
12         couplings for electrically coupling test signals to said selected ones of said  
13    packaging I/O pads corresponding to said sub-set of said particular number and  
14    pattern of chip I/O pads.

- 1       8.     A test module for a production system IC having a particular number and  
2     pattern of chip I/O pads, comprising:  
3         a plurality of test ICs corresponding to a sub-set of a total functionality of said  
4     system IC, each of said plurality of test ICs having a test IC I/O configuration  
5     corresponding to an individual sub-set of said particular number and pattern of chip  
6     I/O pads;  
7         a packaging module designed for said production system IC, having a number  
8     and pattern of packaging system IC pads for receiving said particular number and  
9     pattern of chip I/O pads, said packaging module having packaging I/O pads;  
10        couplings for electrically coupling said test IC I/O configuration of each of  
11     said plurality of test ICs to selected ones of said packaging I/O pads corresponding to  
12     said sub-set of said particular number and pattern of chip I/O pads; and  
13        couplings for electrically coupling test signals to said selected ones of said  
14     packaging I/O pads corresponding to said sub-set of said particular number and  
15     pattern of chip I/O pads.